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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Kie Y. Ahn et al.

Examiner: Phuc T. Dang

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Title: STRUCTURE AND METHOD FOR DUAL GATE OXIDE THICKNESSES

AMENDMENT & RESPONSE

Commissioner for Patents
Washington, D.C. 20231

In response to the Office Action dated April 24, 2002, please amend the application as follows:

IN THE SPECIFICATION

Please make the paragraph substitutions indicated in the appendix entitled Clean Version of Amended Specification Paragraphs. The specific changes incorporated in the substitute paragraphs are shown in the following marked-up versions of the original paragraphs:

Please amend the paragraph of the specification beginning on line 13 of page 12 as follows:

As can be understood from viewing Figure 2, a first transistor 201A formed in thin gate oxide region 212 for use in a logic device has a total dielectric layer of a first thickness, d1. Also as seen from viewing Figure 2 a second transistor 201B formed in the thick gate oxide region 214 for use in a memory device has a total dielectric layer of a second thickness, d2, which is greater than the dielectric layer of the first thickness, d1. The first transistor having a dielectric layer of a first thickness d1 includes a bottom layer 204A of silicon dioxide (SiO₂) and a top layer 206 of silicon nitride (Si₃N₄). The second transistor having a dielectric layer of a second thickness d2 includes a bottom layer 204B of silicon dioxide (SiO₂) and an additional top layer 210 of silicon dioxide (SiO₂). In one embodiment, the first transistor having a dielectric layer of a first thickness d1 includes a dielectric layer of a first thickness d1 which is less than 7 nanometers (nm). In this embodiment, the second transistor having a dielectric layer of a second thickness d2 includes a dielectric layer of a second thickness d2 which is less than 12 nm. In one embodiment, the first transistor having a dielectric layer of a first thickness d1 includes a